INTRODUCTION

The AH1002-DCF DAC Correction Filter (DCF) FPGA core family provides correction in the discrete-time digital domain for the sin(x)/x frequency response of a typical Digital to Analog Converter (DAC).

APPLICATIONS

- Signal Generators
- Modulators
- Test Equipment
- Audio Systems

FEATURES

- Efficient, multiplier-free design minimizes resource utilization and power consumption
- Configurable input and output widths
- Multiple tap-length configurations including 9-tap, 7-tap, and 5-tap
- Arithmetic overflow output monitor
- Clock enable
- Output saturation prevents arithmetic rollover
- Static resettable output
- Registered input, registered output
- Clock rates over 714 MHz supported
- Includes complete simulation and verification software support suite
- Custom designs and configurations available

DESCRIPTION

In sampled systems the DACs used for signal conversion from digital to analog nearly universally include a zero-order hold function of the output analog signal as part of the conversion process. The zero-order hold unavoidably applies a sin(x)/x frequency response to the output signal with the first null at the conversion sample rate frequency. The

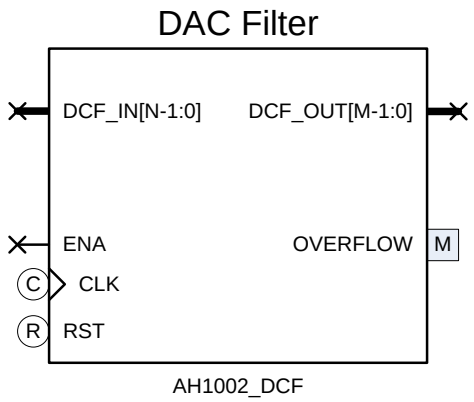

Figure 1. DAC Correction Filter Schematic Symbol

sin(x)/x response of the zero-order hold can be accurately corrected by applying a compensating x/sin(x) response. The AH1002-DCF filter family produces the required compensating response so that the frequency spectrum amplitude of the converted signal is accurately reproduced up to approximately 0.4 times the sampling frequency or higher.

Generally there is a tradeoff between filter complexity and accuracy, and in this case there are practical tradeoffs between the accuracy and extent of the filter response and the number of taps. This allows implementers the ability to manage complexity and performance while still achieving high efficiency.

The implementation complexity of the filters is kept low using Anchor Hill's proprietary design techniques that provide both high accuracy and high implementation efficiency. Multiplier resources are often strained in FPGA designs and the AH1002-DCF filters use no multipliers in order to preserve limited FPGA resources like Xilinx DSP48. Resource utilization for Xilinx targets for the 5-tap filter is shown in Table 1.

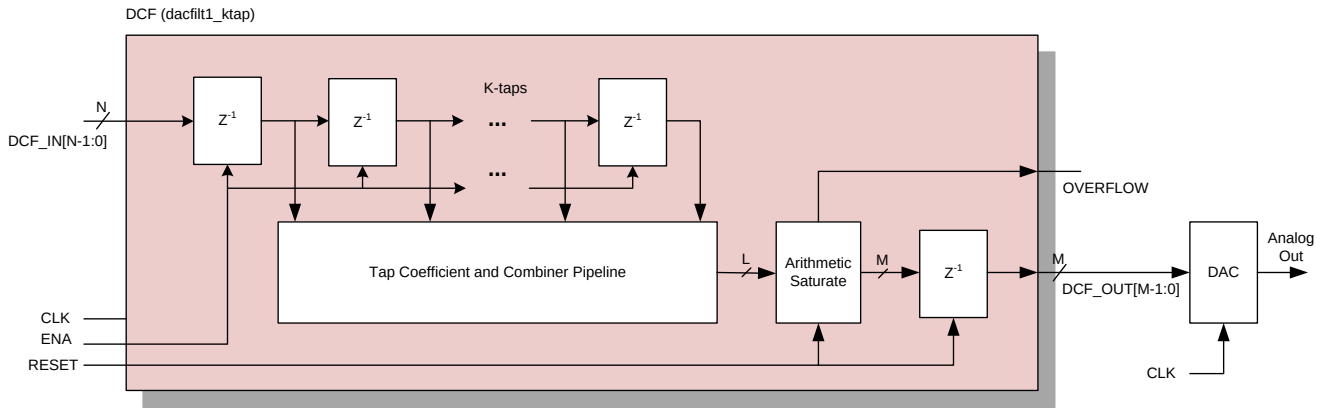

Figure 2. AH1002-DCF block diagram showing integration with a typical Digital to Analog Converter.

Resource Utilization and Speed

The 5-tap DAC Correction Filter has been synthesized with the resource utilizations and speeds shown in Table 1 for the indicated Xilinx device families. Results shown are from the Xilinx XST synthesis tools with trimming disabled and the specific devices selected as indicated. Speeds shown are for -2 parts. Resource utilization for the 7-tap and 9-tap versions of the DCF are available on Anchor Hill's website.

Family	Device	Slice Regs	Slice LUTs	Occupied Slices	LUT-FF Pairs	DSP48	Max Freq (MHz)
Kintex-7	xc7k70t	178	135	41	144	0	707
Spartan-6	xc6slx75t	179	140	43	151	0	350
Virtex-5	Xc5vlx50t	178	117	51	181	0	510
Virtex-6	xc6vlx75t	179	134	41	147	0	647

Table 1. DACfilt1_5tap Resource Utilization for certain Xilinx Device Families

Contact Information

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